

We Claim:

1. A multiplier processing system for performing a group-multiply-and-sum instruction, said system comprising:

means for partitioning each of a plurality of operands into a plurality of symbols, said operands and each of said symbols having a predefined bit width;

means for multiplying symbols of a first operand with symbols of a second operand, each of such multiplications producing a product; and

means for adding each product so as to produce a single scalar result, said scalar result capable of being represented by a bit width which is equal to or less than said predefined bit width of said operands without a reduction in the accuracy of said result.

2. The multiplier processing system for performing a group-multiply-and-sum instruction according to claim 1, wherein the instruction comprises a fixed-point arithmetic operation.

3. The multiplier processing system for performing a group-multiply-and-sum instruction according to claim 1, wherein the instruction comprises a fixed-point arithmetic operation.

4. The multiplier processing system for performing a group-multiply-and-sum instruction according to claim 1, further comprising:

means for including a third operand in the addition of said products.

5. A multiplier processing system for performing a group-multiply-sum-and-add instruction, said system comprising:

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means for partitioning each of a plurality of operands into a plurality of symbols, said operands and each of said symbols having a predefined bit width;

means for multiplying symbols of a first operand with symbols of a second operand, each of such multiplications producing a product; and

5 means for adding each product and a third operand so as to produce a single scalar result, said scalar result capable of being represented by a bit width which is equal to or less than said predefined bit width of said operands without a reduction in the accuracy of said result.

10 6. The multiplier processing system for performing a group-multiply-sum-and-add instruction according to claim 5, wherein the instruction comprises a fixed-point arithmetic operation.

7. The multiplier processing system for performing a group-multiply-sum-and-add instruction according to claim 5, wherein the instruction comprises a fixed-point arithmetic operation.

18. A method for performing a group-multiply-and-sum instruction, said method comprising the steps of:

partitioning each of a plurality of operands into a plurality of symbols, said operands and each of said symbols having a predefined bit width;

multiplying symbols of a first operand with symbols of a second operand, each of such multiplications producing a product; and

adding each product so as to produce a single scalar result, said scalar result capable of being

represented by a bit ~~width~~ which is equal to or less than said ~~predefined~~ bit width of said operands without a reduction in the accuracy of said result.

2/9. The method for performing a group-multiply-and-sum instruction according to claim 8, wherein the instruction comprises a fixed-point arithmetic operation.

5-10 C/ 10. The method for performing a group-multiply-and-sum instruction according to claim 8, wherein the instruction comprises a fixed-point arithmetic operation.

3/11. The method for performing a group-multiply-and-sum instruction according to claim 8, further comprising:

including a third operand in the addition of said products.

6/12. A method for performing a group-multiply-sum-and-add instruction, said method comprising the steps of:

partitioning each of a plurality of operands into a plurality of symbols, said operands and each of said symbols having a predefined bit width;

multiplying symbols of a first operand with symbols of a second operand, each of such multiplications producing a product; and

adding each product and a third operand so as to produce a single scalar result, said scalar result capable of being represented by a bit width which is equal to or less than said predefined bit width of said operands without a reduction in the accuracy of said result.

- 6 7 13. The method for performing a group-multiply-sum-and-add instruction according to claim 12, wherein the instruction comprises a fixed-point arithmetic operation.

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14. The method for performing a group-multiply-sum-and-add instruction according to claim 12, wherein the instruction comprises a fixed-point arithmetic operation.

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